Listing of Claims:

1. (Currently Amended) A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for a device pair comprising ~~of~~ semiconductor devices; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices ~~comprising the device pair~~.

2. (Original) The method of claim 1, wherein the device pair comprises two transistors.

3. (Original) The method of claim 2, wherein the distribution of device mismatch comprises a distribution of Vt (threshold voltage) mismatch.

4. (Currently Amended) The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises retrieving said DC voltage characteristic data from a database.

5. (Currently Amended) The method of claim 1, wherein the semiconductor devices comprise transistors and wherein the step of obtaining DC voltage characteristic data for the device pair comprises measuring subthreshold DC voltage characteristic data in a subthreshold region of the transistors ~~comprising the device pair~~.

6. (Original) The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

7. (Currently Amended) The method of claim 1, further comprising the step of determining a variation in a device characteristic for a device of an integrated circuit comprising the device pair ~~the distribution of variation of device mismatch for the device pair~~.

8. (Currently Amended) The method of claim 7 ~~8~~, further comprising the step of assessing random variation of device mismatch of the semiconductor integrated circuit using

variations in the device characteristic for each device of the integrated circuit as determined from distributions of variation of device mismatch for device pairs within the integrated circuit.

9. (Currently Amended) The method of claim 8, wherein the device characteristic comprises threshold voltage and wherein the ~~devices~~ device pairs comprise transistors.

10. (Currently Amended) A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring transistors in the integrated circuit;

determining a distribution of Vt (threshold voltage) mismatch for a selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

11. (Original) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprises obtaining subthreshold DC voltage characteristic data while biasing the transistors of the device pair in a subthreshold region.

12. (Original) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

13. (Currently Amended)The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises:

(i) serially connecting a first transistor and a second transistor;

(ii) applying a first gate voltage to a gate of the first transistor and a second gate voltage to a gate of the second transistor such that the first and second transistors are biased in a subthreshold voltage region, wherein at least one of the first and second gate voltages comprises a varying input voltage; and

(iii) determining output voltage of a node between the first and second transistors as a function of the varying input voltage~~; and~~

~~(iv) repeating steps (i) - (iii) for each of a plurality of separate device pairs of the first and second transistors.~~

14. (Currently Amended) The method of claim 13, wherein at least one of the first and second gate voltages comprises a constant input voltage to maintain the respective transistor in the subthreshold voltage region.

15. (Original) The method of claim 13, wherein the step of determining a distribution of Vt mismatch for the selected device pair using the corresponding DC voltage characteristic data for the device pair, comprises the steps of:

determining a distribution of V_{IN} for a given output voltage, V_{OUT}; and

determining a distribution of Vt mismatch of the first and second transistors from the distribution of V_{IN}.

16. (Original) The method of claim 15, wherein the distribution of V_{IN} corresponds to a distribution of Vt mismatch between the first and second transistors when the first and second transistors each comprise an NFET.

17. (Original) The method of claim 15, wherein the distribution of V_{IN} corresponds to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

18. (Original) The method of claim 10, wherein the integrated circuit comprises an SRAM (static random access memory) cell.

19. (Original) The method of claim 10, wherein the step of determining a Vt variation of transistors in the integrated circuit comprises determining a standard deviation of Vt variation of the transistors.

20. ~ 25. (Canceled)

26. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for a device pair comprising ~~of~~ semiconductor devices; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices ~~comprising the device pair~~.

27. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring transistors in the integrated circuit;

determining a distribution of Vt (threshold voltage) mismatch for a selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random Vt variation of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

28. (New) The program storage device of claim 26, wherein the device pair comprises two transistors.

29. (New) The program storage device of claim 28, wherein the distribution of device mismatch comprises a distribution of Vt (threshold voltage) mismatch.

30. (New) The program storage device of claim 26, wherein the semiconductor devices comprise transistors and wherein the step of obtaining DC voltage characteristic data for the device pair comprises measuring subthreshold DC voltage characteristic data in a subthreshold region of the transistors.

31. (New) The program storage device of claim 27, wherein the instructions for performing the step of obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprise instructions for obtaining subthreshold DC voltage characteristic data while biasing the transistors of the device pair in a subthreshold region.

32. (New) The program storage device of claim 27, wherein the instructions for performing the step of obtaining DC voltage characteristic data for a selected device pair comprise instructions for separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

33. (New) The program storage device of claim 27, wherein the instructions for obtaining DC voltage characteristic data for a selected device pair comprise instructions for performing the steps of:

(i) serially connecting a first transistor and a second transistor;

(ii) applying a first gate voltage to a gate of the first transistor and a second gate voltage to a gate of the second transistor such that the first and second transistors are biased in a subthreshold voltage region, wherein at least one of the first and second gate voltages comprises a varying input voltage; and

(iii) determining output voltage of a node between the first and second transistors as a function of the varying input voltage.

IN THE SPECIFICATION

Please Amend the Abstract of the Disclosure as follows:

Abstract of the Disclosure

Circuits and methods are provided for measuring and characterizing random variations in device characteristics of semiconductor integrated circuit devices~~, which enable circuit designers to accurately measure and characterize random variations in device characteristics (such as transistor threshold voltage) between neighboring devices resulting from random sources such as dopant fluctuations and line edge roughness, for purposes of integrated circuit design and analysis~~. In one aspect, a method for characterizing random variations in device mismatch (e.g., threshold voltage mismatch) between a pair of devices (e.g., transistors) is performed by obtaining subthreshold DC voltage characteristic data for the device pair, and then determining a distribution in voltage threshold mismatch for the device pair directly from the corresponding subthreshold DC voltage characteristic data. The voltage threshold mismatch distributions of different device pairs of a given circuit design can then be used to determine voltage threshold variations of the constituent circuit devices. The voltage threshold variation of the devices can be used to characterize the random variations of the given circuit.

Please amend the paragraph on page 14, lines 23-25, as follows:

~~Fig. 15 is a diagram~~ Figs. 15a and 15b are diagrams of a testing apparatus according to an embodiment of the invention for measuring device parameters for characterizing device mismatch.

Please amend the paragraph on page 15, lines 2-17, as follows:

In general, circuits and methods according to embodiments of the invention are used for measuring and characterizing random variations in device characteristics of semiconductor integrated circuit devices. More specifically, circuits and methods according to embodiments of the invention enable circuit designers to accurately measure and characterize**[[d]]** random variations in device characteristics (such as transistor threshold voltage (Vt)) resulting from random sources, for purposes of integrated circuit design. Methods and circuits according to embodiments of the invention are preferably implemented for determining variations in Vt mismatch between neighboring MOSFETs of a given circuit being analyzed/designed, such as SRAM cells or other logic devices, and using the determined variations in Vt mismatch to characterize random Vt variation of the given circuit.

Please amend the paragraph on page 18, line 18, through page 19, line 4, as follows:

~~AS~~ As noted above, characterizing device mismatch (e.g., Vt mismatch) between neighboring transistors of a given circuit can be performed using one of the circuits of Figs. 2-4 depending on the transistor types. For example, to characterize the variation in Vt mismatch between two neighboring NFETs of a given circuit design, subthreshold DC voltage characteristic data (Vout vs. Vin) would be measured for each of a plurality of the same/similar circuits comprising device pairs as shown in Fig. 2. The DC data would then be analyzed to determine a distribution of Vin for a given Vout, and a distribution for Vt mismatch would be determined using the measured distribution of Vin.